TEXAS INSTRUMENTS

TPS3779, TPS3780

SBVS250 – APRIL 2015

TPS37xx Dual-Channel, Low-Power, High-Accuracy Voltage Detectors

1 Features

- Two-Channel Detectors in Small Packages
- High-Accuracy Threshold and Hysteresis: 1.0%
- Low Quiescent Current: 2 µA (typ)
- Adjustable Detection Voltage Down to 1.2 V
- Multiple Hysteresis Options:
  - 0.5%, 1%, 5%, and 10%
- Temperature Range: –40°C to 125°C
- Push-Pull (TPS3779) and Open-Drain (TPS3780) Output Options
- Available in µSON and SOT23 Packages

2 Applications

- DSP, Microcontroller, and Microprocessor Applications
- Portable Medical Devices
- Building Automation
- Set-Top Boxes
- Solid-State Drives
- Notebook and Desktop Computers
- Portable and Battery-Powered Products
- Power-Supply Sequencing Applications

3 Description

The TPS3779 and TPS3780 are a family of high-accuracy, two-channel voltage detectors with low-power and small solution size. The SENSE1 and SENSE2 inputs include hysteresis to reject brief glitches, ensuring stable output operation without false triggering. This family offers different factory-set hysteresis options of 0.5%, 1%, 5%, or 10%.

The TPS3779 and TPS3780 have adjustable SENSE inputs that can be configured by an external resistor divider. When the voltage at the SENSE1 or SENSE2 input goes below the falling threshold, OUT1 or OUT2 is driven low, respectively. When SENSE1 or SENSE2 rises above the rising threshold, OUT1 or OUT2 goes high, respectively.

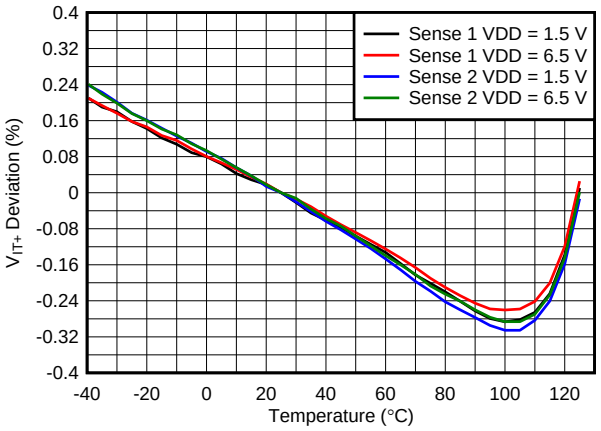
The devices have a very low quiescent current of 2 µA (typical) and provide a precise, space-conscious solution for voltage detection suitable for low-power system-monitoring and portable applications. The TPS3779 and TPS3780 operate from 1.5 V to 6.5 V, over the –40°C to 125°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS37xx	µSON (6)	1.45 mm × 1.00 mm
	SOT23 (6)	2.92 mm × 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Sense Threshold (V_{IT+}) Deviation versus Temperature



Typical Schematic

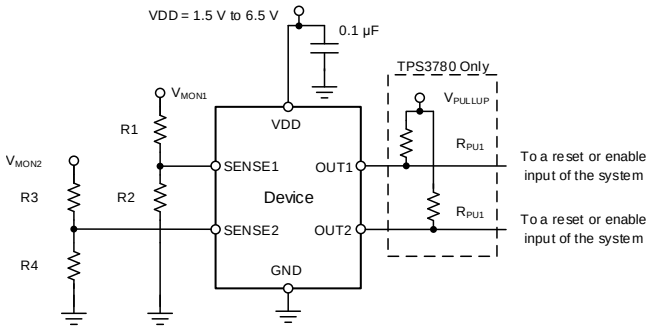


Table of Contents

4 Revision History

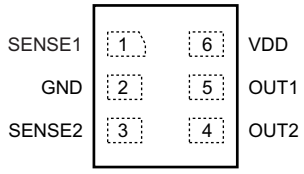
DATE	REVISION	NOTES
April 2015	*	Initial release.

5 Device Comparison Table

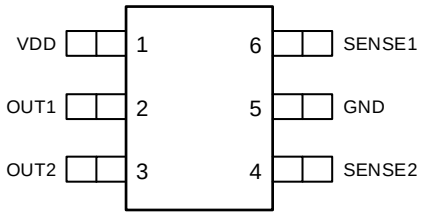
PRODUCT	HYSTERESIS (%)	OUTPUT
TPS3779A	0.5	Push-pull
TPS3779B	5	Push-pull
TPS3779C	10	Push-pull
TPS3779D	1	Push-pull
TPS3780A	0.5	Open-drain
TPS3780B	5	Open-drain
TPS3780C	10	Open-drain
TPS3780D	1	Open-drain

6 Pin Configuration and Functions

DRY Package
1.45-mm × 1-mm µSON
(Top View)



DBV Package
SOT23-6
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DRY	DBV		
GND	2	5	—	Ground
OUT1	5	2	O	OUT1 is the output for SENSE1. OUT1 is asserted (driven low) when the voltage at SENSE1 falls below V_{IT-}. OUT1 is deasserted (goes high) after SENSE1 rises higher than V_{IT+}. OUT1 is a push-pull output for the TPS3779 and an open-drain output for the TPS3780. The open-drain device (TPS3780) can be pulled up to 6.5 V independent of VDD; a pull-up resistor is required for this device.
OUT2	4	3	O	OUT2 is the output for SENSE2. OUT2 is asserted (driven low) when the voltage at SENSE2 falls below V_{IT-}. OUT2 is deasserted (goes high) after SENSE2 rises higher than V_{IT+}. OUT2 is a push-pull output for the TPS3779 and an open-drain output for the TPS3780. The open-drain device (TPS3780) can be pulled up to 6.5 V independent of VDD; a pull-up resistor is required for this device.
SENSE1	1	6	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT1 is asserted.
SENSE2	3	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT2 is asserted.
VDD	6	1	I	Supply voltage input. Connect a 1.5-V to 6.5-V supply to VDD in order to power the device. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin (required for VDD < 1.5 V).

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	7	V
	OUT1, OUT2 (TPS3779 only)	–0.3	VDD + 0.3	V
	OUT1, OUT2 (TPS3780 only)	–0.3	7	V
	SENSE1, SENSE2	–0.3	7	V
Current	OUT1, OUT2		±20	mA
Temperature	Operating junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Power-supply voltage		1.5		6.5	V
	Sense voltage	SENSE1, SENSE2	0		6.5	V
	Output voltage (TPS3779 only)	OUT1, OUT2	0		VDD + 0.3	V
	Output voltage (TPS3780 only)	OUT1, OUT2	0		6.5	V
R_{PU}	Pullup resistor (TPS3780 only)		1.5		10,000	kΩ
	Current	OUT1, OUT2	–5		5	mA
C_{IN}	Input capacitor			0.1		µF
T_J	Junction temperature		–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS3779, TPS3780		UNIT
		DRY (USON)	DBV (SOT23-6)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	306.7	193.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	174.1	134.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	173.4	39.0	
ψ_{JT}	Junction-to-top characterization parameter	30.9	30.4	
ψ_{JB}	Junction-to-board characterization parameter	171.6	38.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	65.2	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, .

7.5 Electrical Characteristics

All specifications are over the operating temperature range of –40°C < T_J < 125°C and 1.5 V ≤ VDD ≤ 6.5 V, unless otherwise noted. Typical values are at T_J = 25°C and VDD = 3.3 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VDD	Input supply range			1.5		6.5	V
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL} (max) = 0.2 V, I_{OL} = 15 µA				0.8	V
I_{DD}	Supply current (into VDD pin)	VDD = 3.3 V, no load, –40°C < T_J < 85°C			2.09	3.72	µA
		VDD = 3.3 V, no load, –40°C < T_J < 125°C				5.80	µA
		VDD = 6.5 V, no load, –40°C < T_J < 85°C			2.29	4.00	µA
		VDD = 6.5 V, no load, –40°C < T_J < 125°C				6.50	µA
V_{IT+}	Positive-going input threshold voltage	$V_{(SENSE)}$ rising			1.194		V
				–1%		1%	
$V_{IT–}$	Negative-going input threshold voltage	$V_{(SENSE)}$ falling	TPS37xxA (0.5% hysteresis)		1.188		V
			TPS37xxB (5% hysteresis)		1.134		V
			TPS37xxC (10% hysteresis)		1.074		V
			TPS37xxD (1% hysteresis)		1.182		V
		$V_{(SENSE)}$ falling		–1%		1%	
$I_{(SENSE)}$	Input current	$V_{(SENSE)}$ = 0 V or VDD		–15		15	nA
V_{OL}	Low-level output voltage	VDD ≥ 1.2 V, I_{SINK} = 0.4 mA				0.25	V
		VDD ≥ 2.7 V, I_{SINK} = 2 mA				0.25	V
		VDD ≥ 4.5 V, I_{SINK} = 3.2 mA				0.30	V
V_{OH}	High-level output voltage (TPS3779 only)	VDD ≥ 1.5 V, I_{SOURCE} = 0.4 mA		0.8 VDD			V
		VDD ≥ 2.7 V, I_{SOURCE} = 1 mA		0.8 VDD			V
		VDD ≥ 4.5 V, I_{SOURCE} = 2.5 mA		0.8 VDD			V
$I_{lkg(OD)}$	Open-drain output leakage current (TPS3780 only)	High impedance, $V_{(SENSE)}$ = $V_{(OUT)}$ = 6.5 V, –40°C < T_J < 85°C		–50		50	nA
		High impedance, $V_{(SENSE)}$ = $V_{(OUT)}$ = 6.5 V, –40°C < T_J < 125°C		–250		250	nA

(1) Outputs are undetermined below $V_{(POR)}$.

7.6 Timing Requirements

Typical values are at T_J = 25°C and VDD = 3.3 V. SENSE transitions between 0 V and 1.3 V.

		MIN	NOM	MAX	UNIT
$t_{PD(r)}$	SENSE (rising) to OUT propagation delay		5.5		µs
$t_{PD(f)}$	SENSE (falling) to OUT propagation delay		10		µs
t_{SD}	Startup delay(1)		570		µs

(1) During power-on or a VDD transient below VDD(min), the outputs reflect the input conditions 570 µs after VDD transitions through VDD(min).

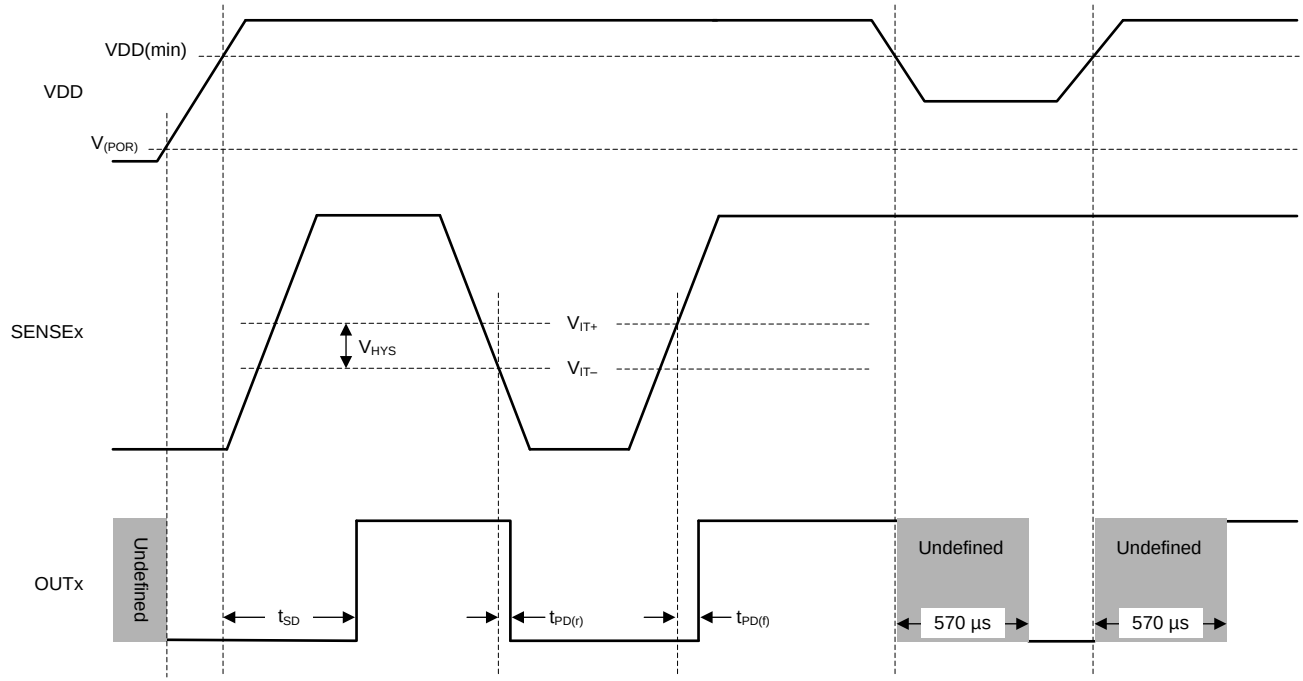


Figure 1. Timing Diagram

7.7 Typical Characteristics

At T_J = 25°C with a 0.1-µF capacitor close to VDD, unless otherwise noted.

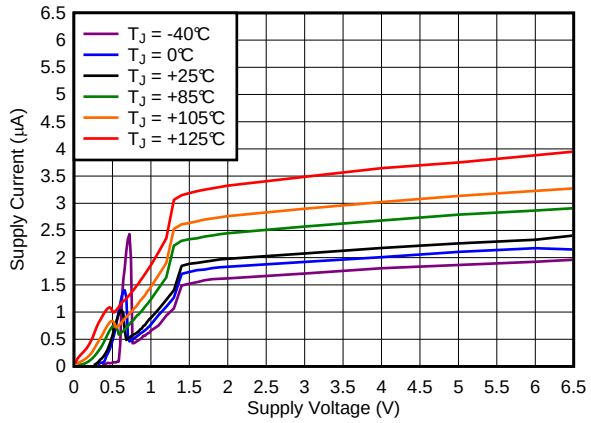


Figure 2. Supply Current vs Supply Voltage

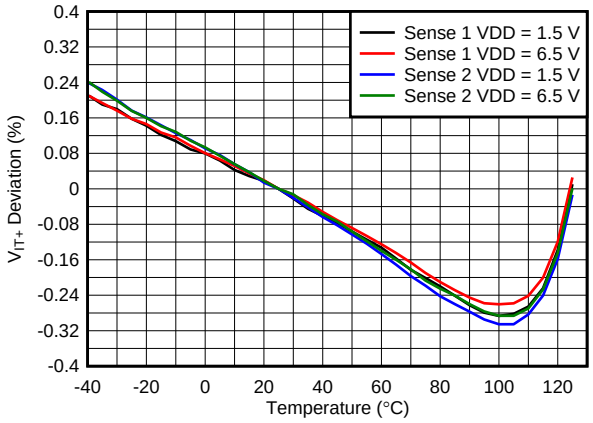


Figure 3. Sense Threshold (V_{IT+}) Deviation vs Temperature

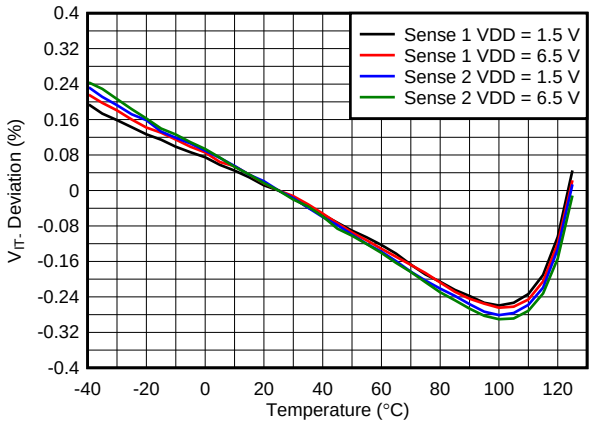


Figure 4. Sense Threshold (V_{IT-}) Deviation vs Temperature

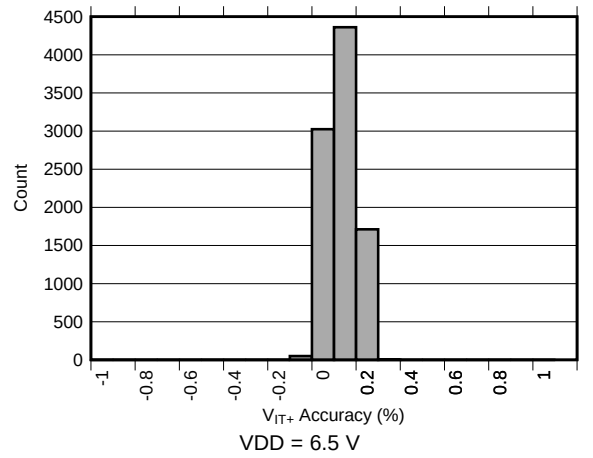


Figure 5. Sense Threshold (V_{IT+})

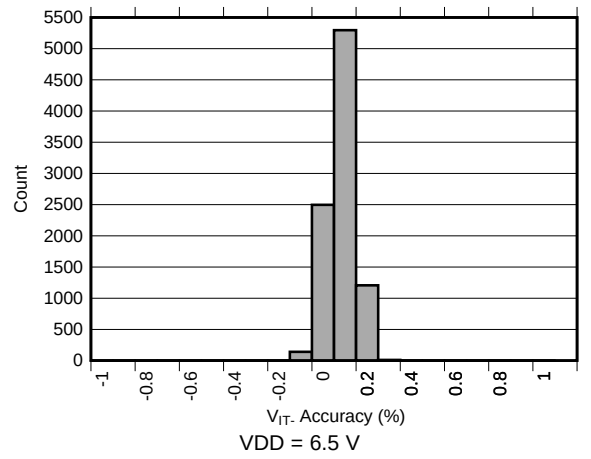


Figure 6. Sense Threshold (V_{IT-})

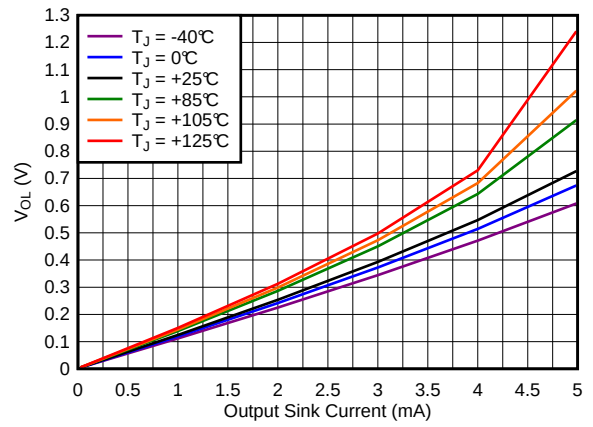


Figure 7. Output Voltage Low vs Output Current (VDD = 1.5 V)

Typical Characteristics (continued)

At T_J = 25°C with a 0.1-µF capacitor close to VDD, unless otherwise noted.

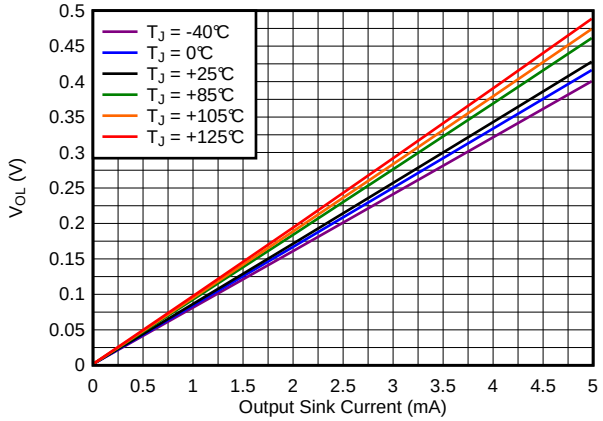


Figure 8. Output Voltage Low vs Output Current (VDD = 3.3 V)

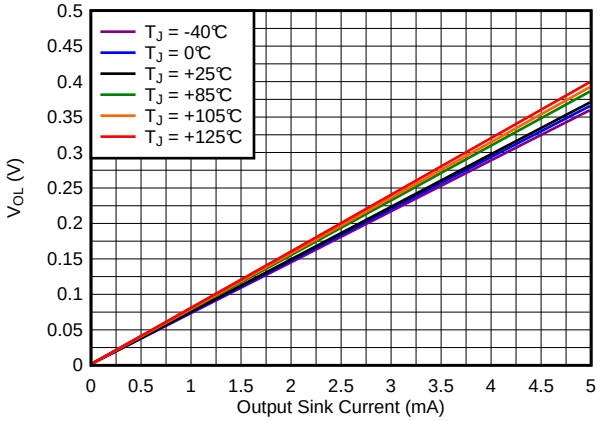


Figure 9. Output Voltage Low vs Output Current (VDD = 6.5 V)

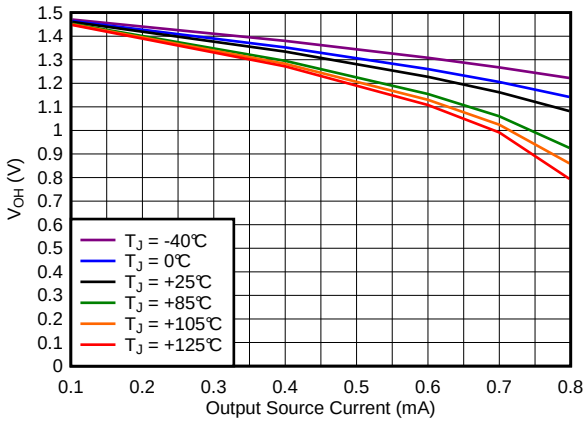


Figure 10. Output Voltage High vs Output Current (VDD = 1.5 V)

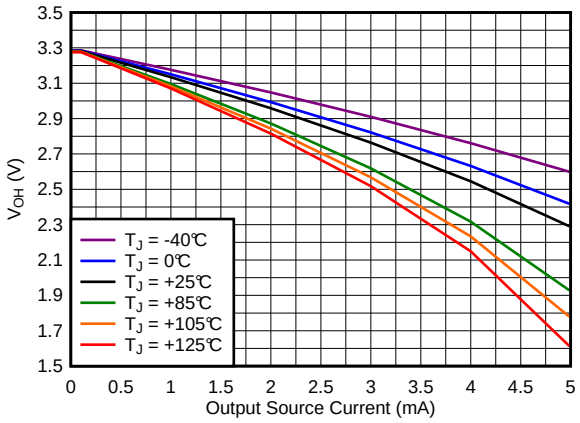


Figure 11. Output Voltage High vs Output Current (VDD = 3.3 V)

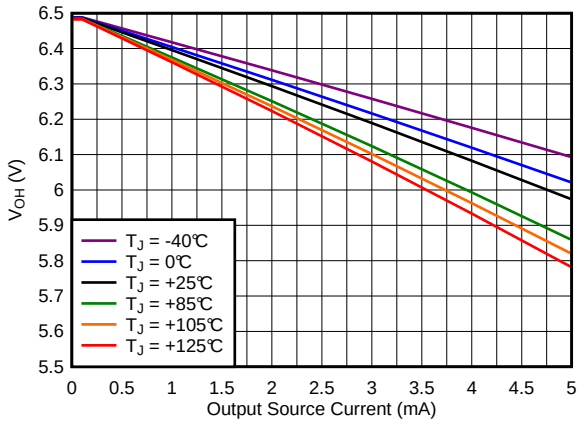
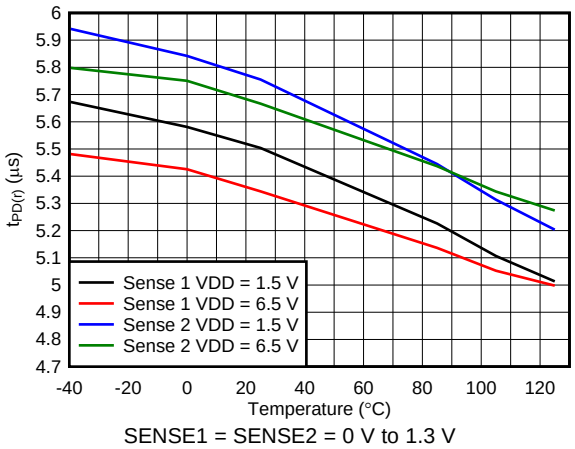


Figure 12. Output Voltage High vs Output Current (VDD = 6.5 V)

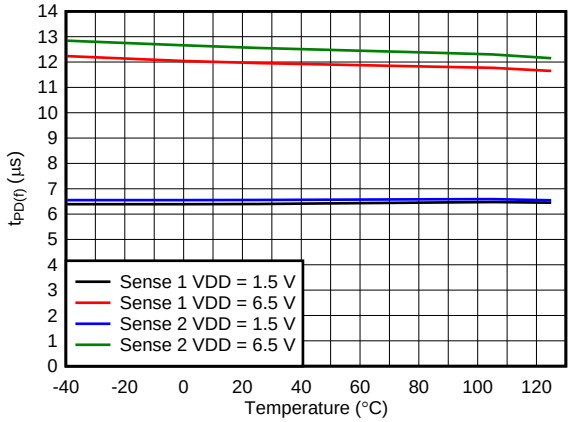


SENSE1 = SENSE2 = 0 V to 1.3 V

Figure 13. Propagation Delay from Sense High to Output High

Typical Characteristics (continued)

At T_J = 25°C with a 0.1-µF capacitor close to VDD, unless otherwise noted.



SENSE1 = SENSE2 = 1.3 V to 0 V

Figure 14. Propagation Delay from Sense Low to Output Low

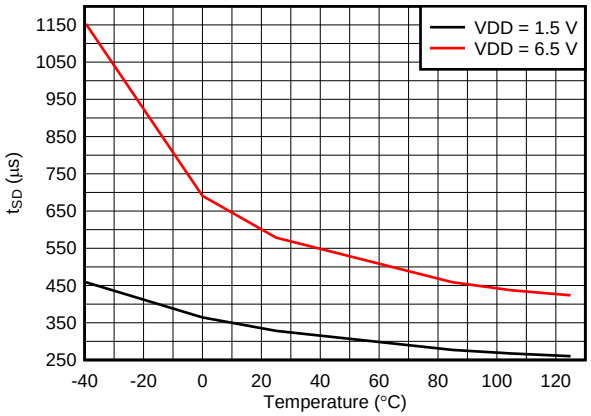
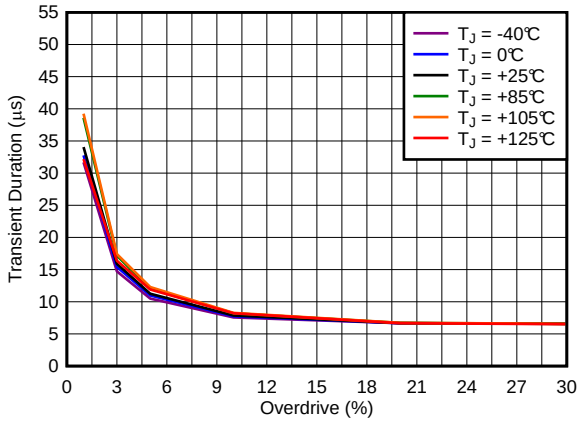
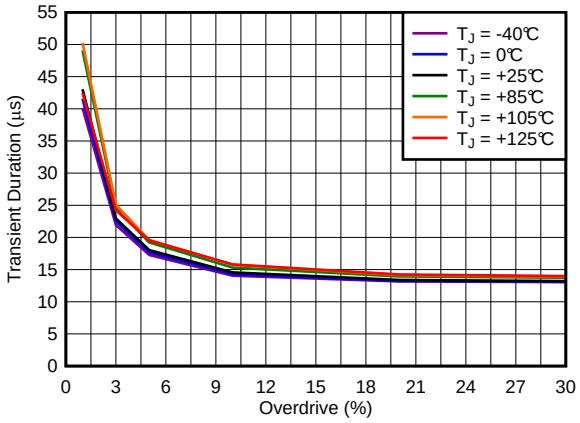


Figure 15. Startup Delay



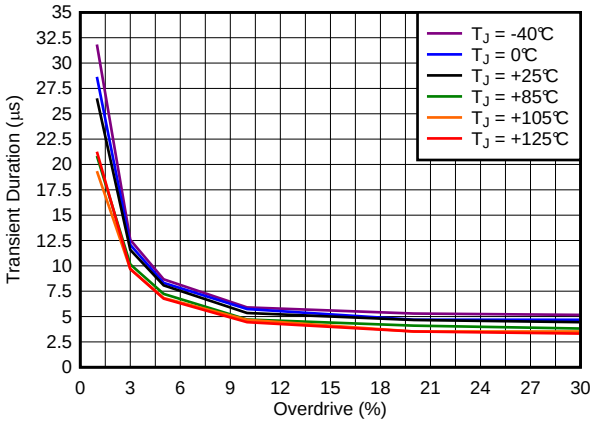
High-to-low transition occurs above the curve

Figure 16. Minimum Transient Duration (HL) vs Overdrive (VDD = 1.5 V)



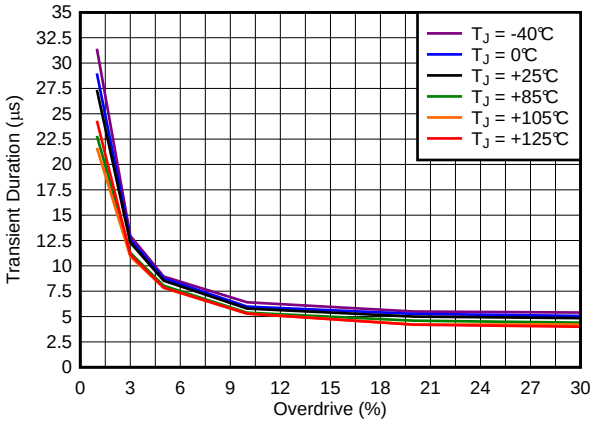
High-to-low transition occurs above the curve

Figure 17. Minimum Transient Duration (HL) vs Overdrive (VDD = 6.5 V)



Low-to-high transition occurs above the curve

Figure 18. Minimum Transient Duration (LH) vs Overdrive (VDD = 1.5 V)



Low-to-high transition occurs above the curve

Figure 19. Minimum Transient Duration (LH) vs Overdrive (VDD = 6.5 V)

8 Detailed Description

8.1 Overview

The TPS3779 and TPS3780 are a family of small, low quiescent current (I_{DD}), dual-channel voltage detectors. These devices have high-accuracy, rising and falling input thresholds, and assert the output as shown in Table 1. The output (OUTx pin) goes low when the SENSEx pin is less than V_{IT-} and goes high when the pin is greater than V_{IT+}. The TPS3779 and TPS3780 offer multiple hysteresis options from 0.5% to 10% for use in a wide variety of applications. These devices have two independent voltage detection channels that can be used in systems where multiple voltage rails are required to be monitored, or where one channel can be used as an early warning signal and the other channel used as the system reset signal.

Table 1. TPS3779, TPS3780 Truth Table

CONDITIONS	OUTPUT
SENSE1 < V_{IT-}	OUT1 = low
SENSE2 < V_{IT-}	OUT2 = low
SENSE1 > V_{IT+}	OUT1 = high
SENSE2 > V_{IT+}	OUT2 = high

8.2 Functional Block Diagrams

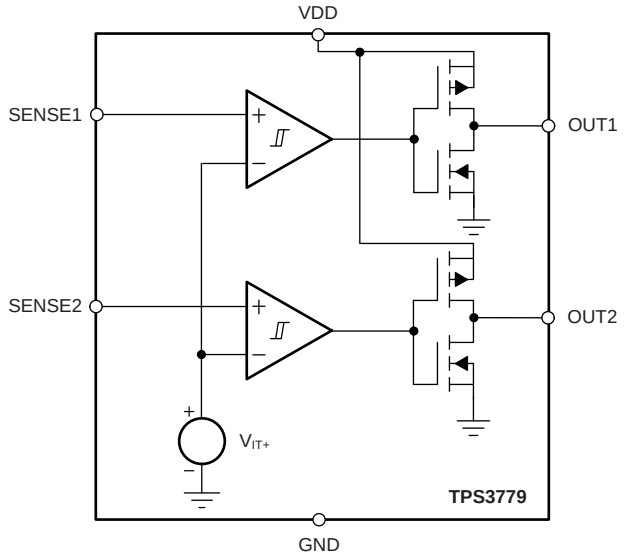


Figure 20. TPS3779 Block Diagram

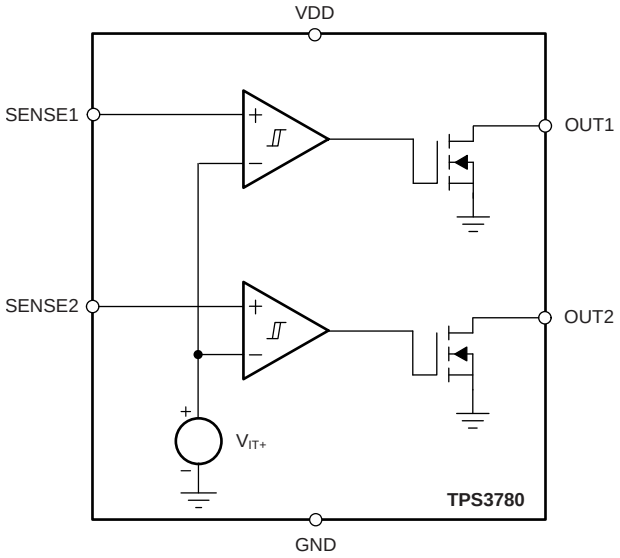


Figure 21. TPS3780 Block Diagram

8.3 Feature Description

8.3.1 Inputs (SENSE1, SENSE2)

The TPS3779 and TPS3780 have two comparators for voltage detection. Each comparator has one external input; the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to V_{IT+} and the falling threshold is trimmed to be equal to $V_{IT–}$. The built-in falling hysteresis options make the devices immune to supply rail noise and ensure stable operation.

The comparator inputs can swing from ground to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, for extremely noisy applications, good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the comparator input in order to reduce sensitivity to transients and layout parasitic.

For each SENSE input, the corresponding output (OUTx) is driven to logic low when the input voltage drops below $V_{IT–}$. When the voltage exceeds V_{IT+}, the output (OUTx) is driven high; see Figure 1.

8.3.2 Outputs (OUT1, OUT2)

In a typical device application, the outputs are connected to a reset or enable input of another device, such as a digital signal processor (DSP), central processing unit (CPU), field-programmable gate array (FPGA), or application-specific integrated circuit (ASIC); or the outputs are connected to the enable input of a voltage regulator, such as a dc-dc or low-dropout (LDO) regulator.

The TPS3779 provides two push-pull outputs. The logic high level of the outputs is determined by the VDD pin voltage. With this configuration pull-up resistors are not required, thus saving board space. However, all interface logic levels must be examined. All OUT connections must be compatible with the VDD pin logic level.

The TPS3780 provides two open-drain outputs (OUT1 and OUT2); pull-up resistors must be used to hold these lines high when the output goes to a high-impedance condition (not asserted). By connecting pull-up resistors to the proper voltage rails, the outputs can be connected to other devices at correct interface voltage levels. The outputs can be pulled up to 6.5 V, independent of the device supply voltage. To ensure proper voltage levels, make sure to choose the correct pull-up resistor values. The pull-up resistor value is determined by V_{OL}, the sink current capability, and the output leakage current ($I_{lkg(OD)}$). These values are specified in the *Electrical Characteristics* table. By using wired-AND logic, OUT1 and OUT2 can be combined into one logic signal. The *Inputs (SENSE1, SENSE2)* section describes how the outputs are asserted or deasserted. See Figure 1 for a description of the relationship between threshold voltages and the respective output.

8.4 Device Functional Modes

8.4.1 Normal Operation (VDD ≥ VDD(min))

When the voltage on VDD is greater than VDD(min) for t_{SD}, the output signals react to the present state of the corresponding SENSE pins.

8.4.2 Power-On Reset (VDD < $V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the logic low output to GND ($V_{(POR)}$), both outputs are undefined and are not to be relied upon for proper system function.

9 Application and Implementation

9.1 Application Information

The TPS3779 and TPS3780 are used as precision dual-voltage detectors. The monitored voltage, VDD voltage, and output pullup voltage (TPS3780 only) can be independent voltages or connected in any configuration.

9.1.1 Threshold Overdrive

Threshold overdrive is how much VDD exceeds the specified threshold, and is important to know because smaller overdrive results in slower OUTx response. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 1:

$$\text{Overdrive} = | (\text{VDD} / V_{IT} - 1) \times 100\% | \quad (1)$$

where

- V_{IT} is either V_{IT-} or V_{IT+}, depending on whether calculating the overdrive for the negative-going threshold or the positive-going threshold, respectively.

Figure 16 illustrates the VDD minimum detectable pulse versus overdrive, and is used to visualize the relationship overdrive has on $t_{PD(f)}$ for negative-going events.

9.1.2 Sense Resistor Divider

The resistor divider values and target threshold voltage can be calculated by using Equation 2 and Equation 3 to determine $V_{MON(UV)}$ and $V_{MON(PG)}$, respectively.

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT-} \quad (2)$$

$$V_{MON(PG)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT+} \quad (3)$$

where

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins,
- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected, and
- $V_{MON(PG)}$ is the target voltage at which the output goes high when V_{MONx} rises.

Choose R_{TOTAL} (= R1 + R2) so that the current through the divider is approximately 100 times higher than the input current at the SENSEx pins. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, refer to application report SLVA450, *Optimizing Resistor Dividers at a Comparator Input*, available for download from www.ti.com.

9.2 Typical Applications

9.3 Monitoring Two Separate Rails

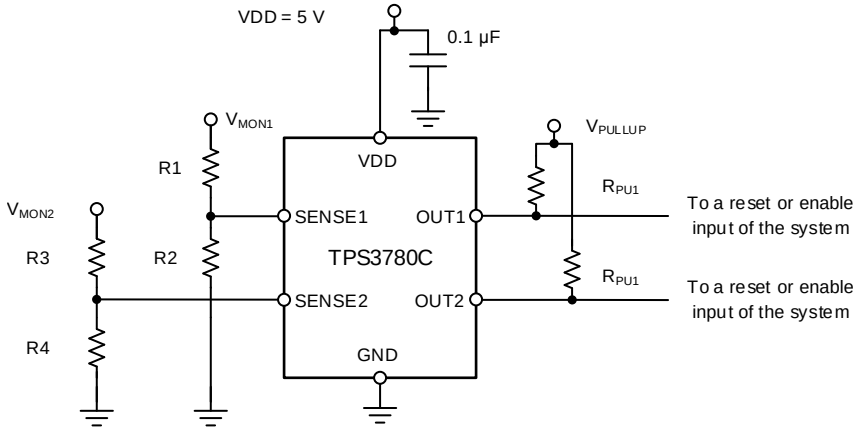


Figure 22. Monitoring Two Separate Rails Schematic

9.3.1 Design Requirements

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
VDD	5 V	5 V
Hysteresis	10%	10%
Monitored voltage 1	3.3 V nominal, $V_{MON(PG)}$ = 2.9 V, $V_{MON(UV)}$ = 2.6 V	$V_{MON(PG)}$ = 2.908 V, $V_{MON(UV)}$ = 2.618 V
Monitored voltage 2	3 V nominal, $V_{MON(PG)}$ = 2.6 V, $V_{MON(UV)}$ = 2.4 V	$V_{MON(PG)}$ = 2.606 V, $V_{MON(UV)}$ = 2.371 V
Output logic voltage	3.3-V CMOS	3.3-V CMOS

9.3.2 Detailed Design Procedure

1. Select the TPS3780C. The C version is selected to satisfy the hysteresis requirement. The TPS3780 is selected for the output logic requirement. An open-drain output allows for the output to be pulled up to a voltage other than VDD.
2. The resistor divider values are calculated by using Equation 2 and Equation 3. For SENSE1, R1 = 1.13 MΩ and R2 = 787 kΩ. For SENSE2, R3 (R1) = 681 kΩ and R4 (R2) = 576 kΩ.

9.3.3 Application Curve

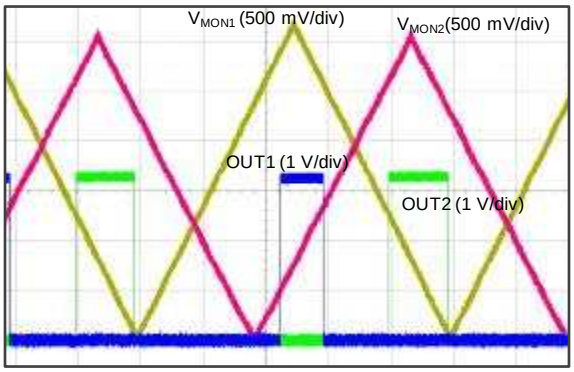


Figure 23. Monitoring Two Separate Rails Curve

9.4 Early Warning Detection

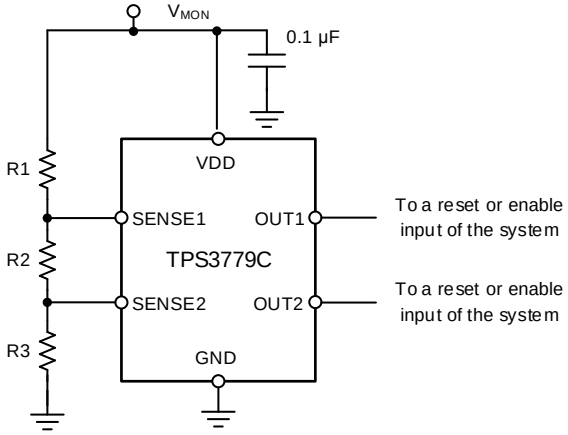


Figure 24. Early Warning Detection Schematic

9.4.1 Design Requirements

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
VDD	V_{MON}	V_{MON}
Hysteresis	10%	10%
Monitored voltage 1	$V_{MON(PG)}$ = 3.3 V, $V_{MON(UV)}$ = 3 V	$V_{MON(PG)}$ = 3.330 V, $V_{MON(UV)}$ = 2.997 V
Monitored voltage 2	$V_{MON(PG)}$ = 3.9 V, $V_{MON(UV)}$ = 3.5 V	$V_{MON(PG)}$ = 3.921 V, $V_{MON(UV)}$ = 3.529 V

9.4.2 Detailed Design Procedure

1. Select the TPS3779C. The C version is selected to satisfy the hysteresis requirement. The TPS3779 is selected to save on component count and board space.
2. Use Equation 4 to calculate the total resistance for the resistor divider. Determine the minimum total resistance of the resistor network necessary to achieve the current consumption specification. For this example, the current flow through the resistor network is chosen to be 1.41 µA. Use the key transition point for V_{MON2}. For this example, the low-to-high transition, $V_{MON(PG)}$, is considered more important.

$$R_{TOTAL} = \frac{V_{MON(PG\_2)}}{I} = \frac{3.9\ V}{1.41\ \mu A} = 2.78\ M\Omega \quad (4)$$

   where
   - $V_{MON(PG\_2)}$ is the target voltage at which OUT2 goes high when V_{MON2} rises, and
   - I is the current flowing through the resistor network.

3. After R_{TOTAL} is determined, R3 can be calculated using Equation 5. Select the nearest 1% resistor value for R3. In this case, 845 kΩ is the closest value.

$$R3 = \frac{V_{IT+}}{I} = \frac{1.194\ V}{1.41\ \mu A} = 846\ k\Omega \quad (5)$$

4. Use Equation 6 to calculate R2. Select the nearest 1% resistor value for R2. In this case, 150 kΩ is the closest value. Use the key transition point for V_{MON1}. For this example, the low-to-high transition, $V_{MON(UV)}$, is considered more important.

$$R2 = \frac{R_{TOTAL}}{V_{MON(UV\_1)}} \bullet V_{IT-} - R3 = \frac{2.78\ M\Omega}{3\ V} \bullet 1.074\ V - 845\ k\Omega = 149\ k\Omega \quad (6)$$

   where
   - $V_{MON(UV\_1)}$ is the target voltage at which OUT1 goes low when V_{MON1} falls.

5. Use Equation 7 to calculate R1. Select the nearest 1% resistor value for R1. In this case, 1.78 MΩ is a 1% resistor.

$$R1 = R_{TOTAL} - R2 - R3 = 2.78\ M\Omega - 150\ k\Omega - 845\ k\Omega = 1.78\ M\Omega \quad (7)$$

9.4.3 Application Curve

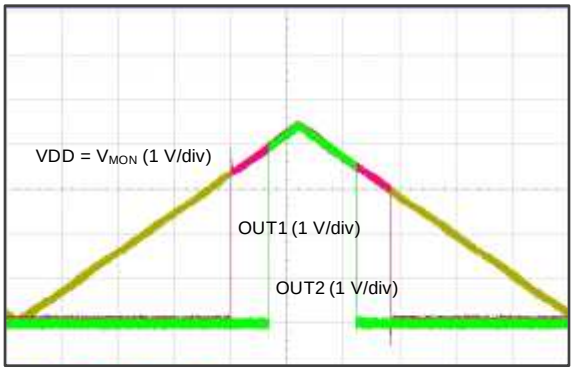


Figure 25. Early Warning Detection Curve

10 Power-Supply Recommendations

The TPS3779 and TPS3780 are designed to operate from an input voltage supply range between 1.5 V and 6.5 V. An input supply capacitor is not required for this device; however, good analog practice (required for less VDD < 1.5 V) is to place a 0.1-µF or greater capacitor between the VDD pin and the GND pin. This device has a 7-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.

For applications where SENSE is greater than 0 V before VDD, and subject to a startup slew rate of less than 200 mV per 1 ms, the output can be driven to logic high in error. To correct the output, cycle the SENSE lines below V_{IT-} or sequence SENSE after VDD.

11 Layout

11.1 Layout Guidelines

Place the VDD decoupling capacitor close to the device.

Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum VDD voltage.

11.2 Layout Example

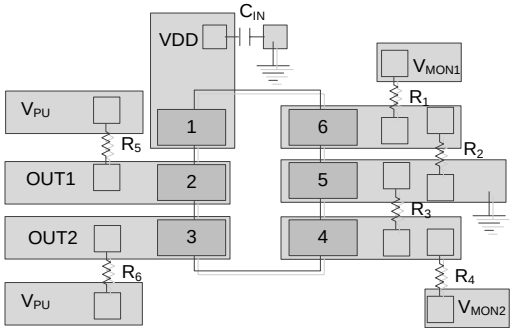


Figure 26. Example SOT23 Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS3779 and TPS3780. SLVU796 details the design kits and evaluation modules for TPS3780EVM-154.

The EVM can be requested at the Texas Instruments web site through the TPS3779 and TPS3780 product folders, or purchased directly from the TI eStore.

12.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS3779 and TPS3780 is available through the respective device product folders under *Simulation Models*.

12.1.2 Device Nomenclature

The TPS3779xyyyz and TPS3780xyyyz are the generic naming conventions for these devices. The TPS3779 and TPS3780 represent the family of these devices; x is used to display the hysteresis version, yyy is reserved for the package designator, and z is the package quantity.

- Example: TPS3779CDBVR
- Family: TPS3779 (push-pull)
- Hysteresis: 10%
- DBV Package: 6-pin SOT
- Package Quantity: R is for a reel (3000 pieces)

12.2 Documentation Support

12.2.1 Related Documentation

12.2.1.1 Related Documentation

For related documentation see the following:

- *TPS3780EVM-154 Evaluation Module*, SLVU796
- Application report SLVA450—*Optimizing Resistor Dividers at a Comparator Input*

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS3779	Click here	Click here	Click here	Click here	Click here
TPS3780	Click here	Click here	Click here	Click here	Click here

12.4 Trademarks

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3780ADBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PE8Q	Samples
TPS3780ADBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PE8Q	Samples
TPS3780ADRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(GJ ~ ZU)	Samples
TPS3780ADRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(GJ ~ ZU)	Samples
TPS3780BDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PE9Q	Samples
TPS3780BDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PE9Q	Samples
TPS3780BDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZV	Samples
TPS3780BDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZV	Samples
TPS3780CDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PF1Q	Samples
TPS3780CDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PF1Q	Samples
TPS3780CDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZW	Samples
TPS3780CDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZW	Samples
TPS3780DDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PF2Q	Samples
TPS3780DDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PF2Q	Samples
TPS3780DDRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZX	Samples
TPS3780DDRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

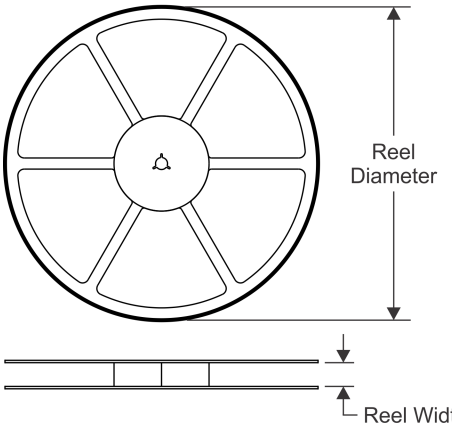
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

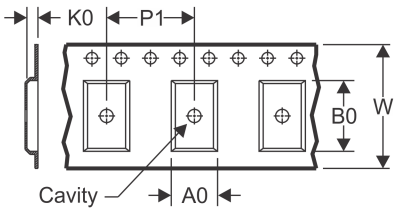
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

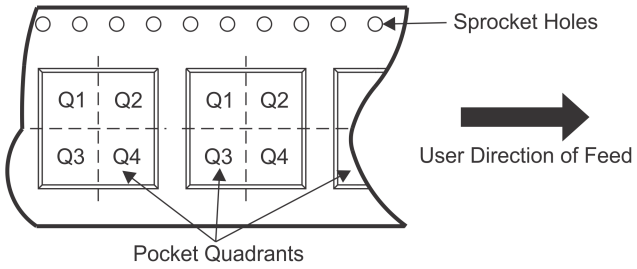


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

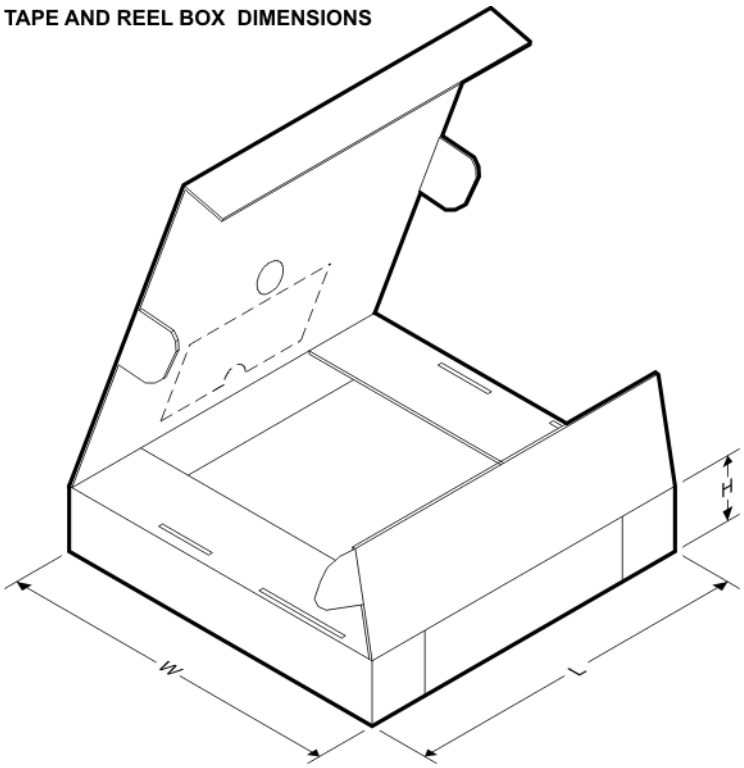
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3780ADBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780ADBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780ADRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS3780ADRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS3780BDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780BDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780BDRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS3780BDRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS3780CDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780CDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780CDRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS3780CDRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS3780DDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780DDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780DDRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
TPS3780DDRYT	SON	DRY	6	250	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1

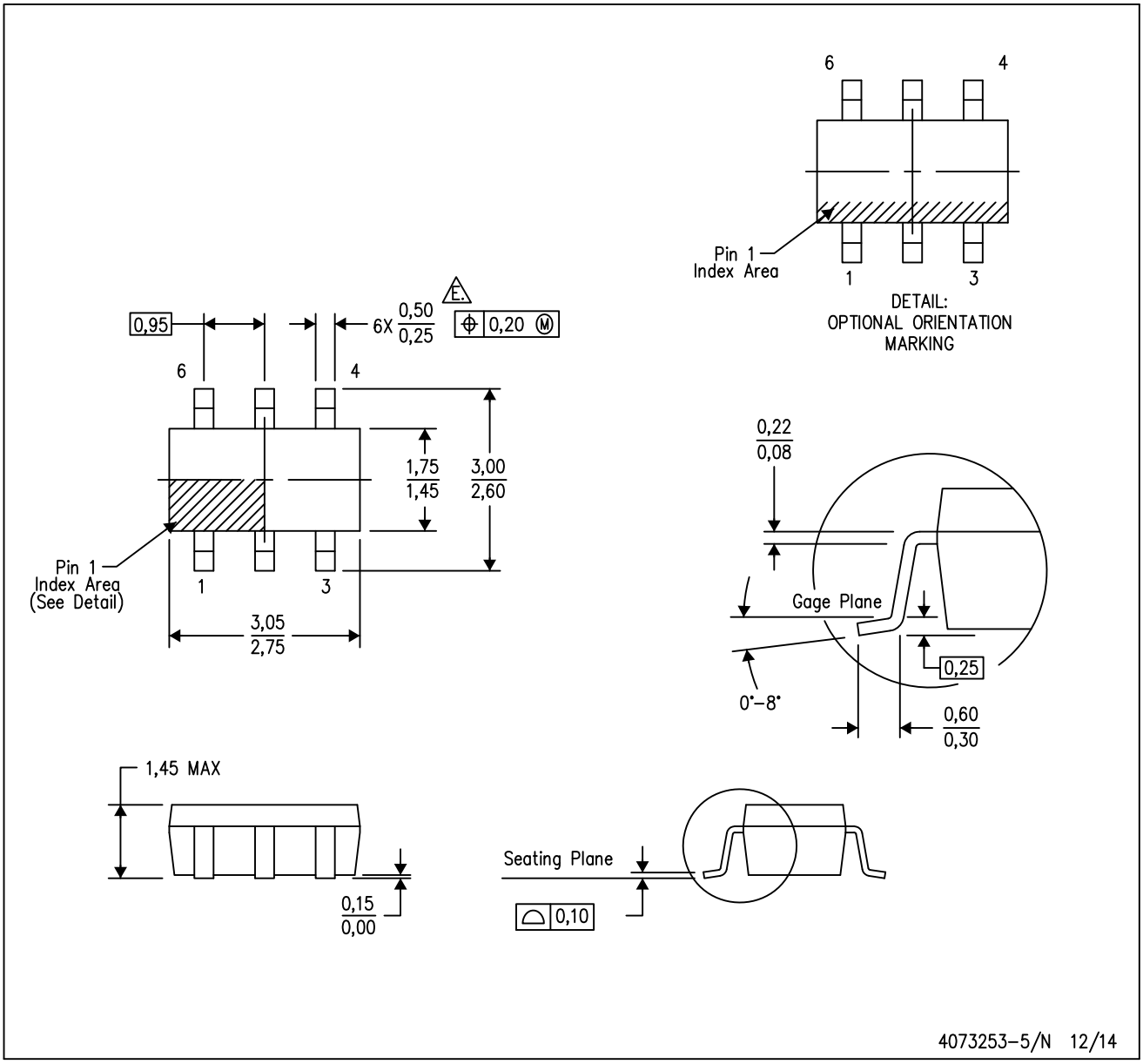
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

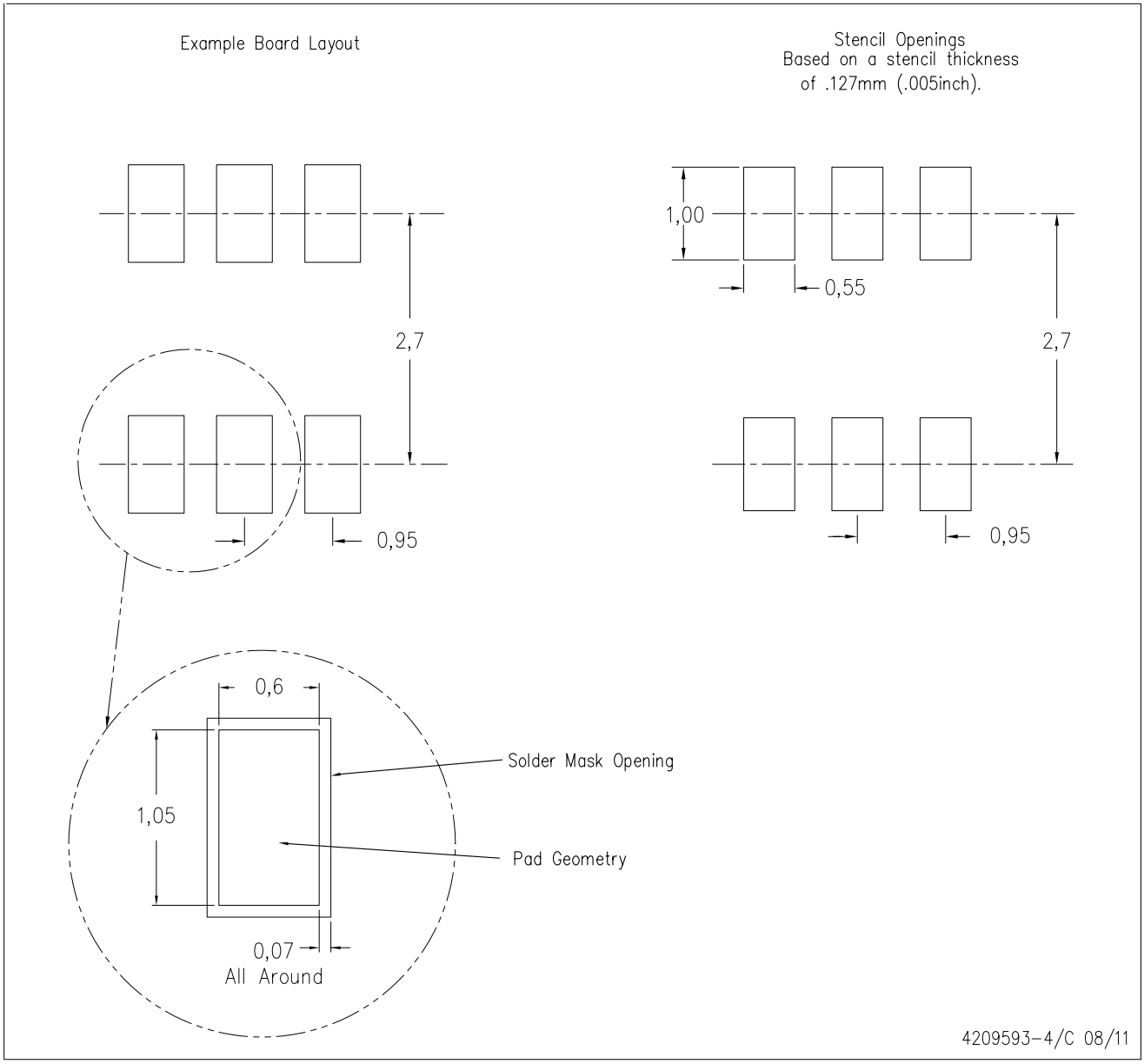
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3780ADBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780ADBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3780ADRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS3780ADRYT	SON	DRY	6	250	202.0	201.0	28.0
TPS3780BDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780BDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3780BDRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS3780BDRYT	SON	DRY	6	250	202.0	201.0	28.0
TPS3780CDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780CDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3780CDRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS3780CDRYT	SON	DRY	6	250	202.0	201.0	28.0
TPS3780DDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780DDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3780DDRYR	SON	DRY	6	5000	202.0	201.0	28.0
TPS3780DDRYT	SON	DRY	6	250	202.0	201.0	28.0

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



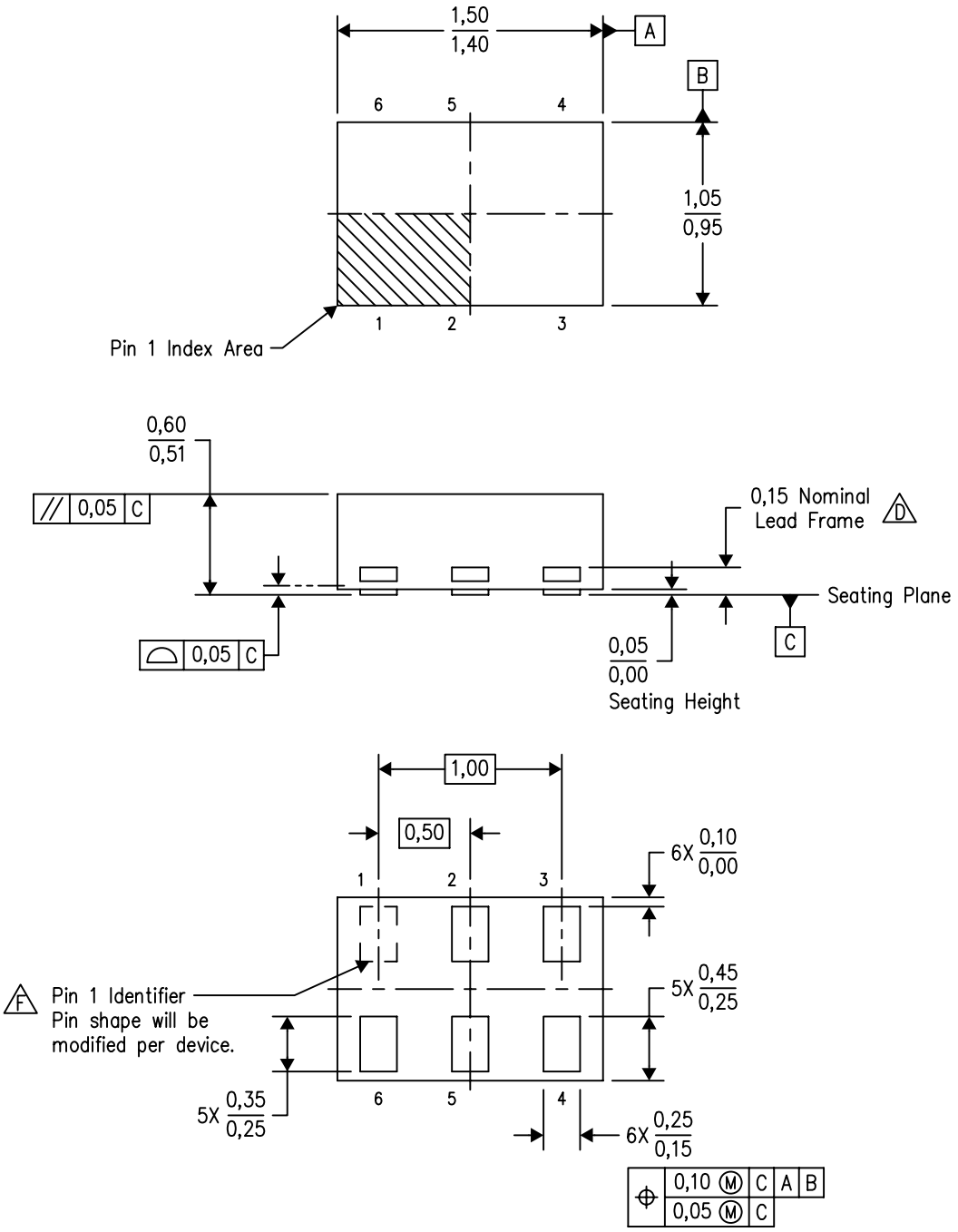
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

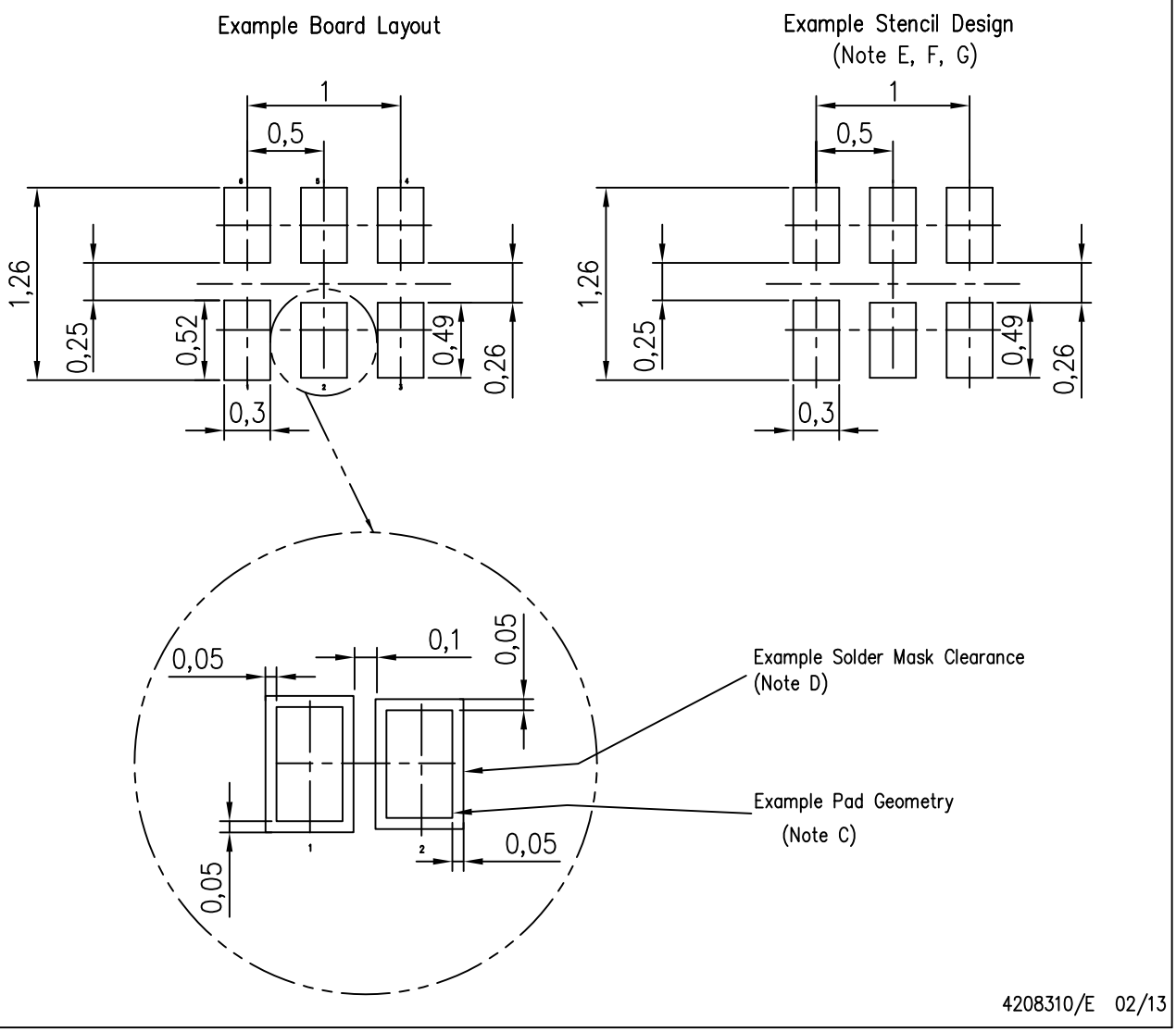
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4207181/F 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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